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SEARCH REQUEST FORM Scientific and Technical Information Center - EIC2800

Rev. 1/26/2006 This is an experimental format -- Please give suggestions or comments to Jeff Harrison, JEF-4B68, 22511.

Date 7/9/06 Serial # 10/804,737 Priority Application Date 3/18/04Your Name M. Lewis Examiner # _____AU 2522 Phone 272-7838 Room 5A30In what format would you like your results? Paper is the default. PAPER DISK EMAIL

If submitting more than one search request form, please prioritize the searches in order of need.

Where have you searched so far on this case?

Circle: USPT DWPI EPO Abs JPO Abs IBM TDB

Other: _____

What relevant art have you found so far? Please attach citations or Information Disclosure Statements.

What types of references would you like? Please checkmark:

Primary Refs ☒ Nonpatent Literature _____ Teaching Refs _____
Secondary Refs ☒ Foreign Patents _____ Other _____Is this a "Fast & Focused Search" request? (Circle One) YES NOA "Fast & Focused Search" is completed in 2-3 hours (maximum). The search must be on a very specific topic and meet certain criteria. The criteria are posted in EIC2800 and on the STIC NPL Web Page at <http://uspto-a-patrr-2/siraapps/stic/npl/nplsearch.htm>

What is the topic, such as the novelty, motivation, utility, or other specific facets defining the desired focus of this search? Please include the concepts, synonyms, keywords, acronyms, registry numbers, definitions, structures, strategies, and anything else that helps to describe the topic. Please attach a copy of the abstract and pertinent claims.

Claims 1-20
Active Substrate/Passive SubstrateProblems: See pages 1-4
Solutions: " " 5-6US 6,642,617**Staff Use Only**Searcher: Paul KimSearcher Phone: 2-8949

Searcher Location: STIC-EIC2800, JEF-4B68

Date Searcher Picked Up: 7/17/06Date Completed: 7/26/06Searcher Prep/Rev Time: 4 hrsOnline Time: 1 hrs**Type of Search**

Structure (#) _____

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Other _____

VendorsSTN /Dialog /Questel/Orbit /Lexis-Nexis /WWW/Internet /

Other _____

Reconnected in file 2 21jul06 10:25:35

File 2:INSPEC 1898-2006/Jul W2
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Set	Items	Description
S1	17699	ACTIVE AND PASSIVE
S2	445062	CHIP? ? OR MICROCHIP? ? OR MICRO () CHIP? ? OR DIE OR DIES OR SUBSTRATE? ? OR WAFER? ?
S3	1025008	INTRA OR SAME OR WITHIN
S4	122	INTRACHIP? ? OR INTRADIE? ? OR INTRAWAFER? ? OR INTRASUBST- RATE? ?
S5	232	INTRA () CHIP? ? OR INTRA () DIE? ? OR INTRA () WAFER? ? OR INTRA () SUBSTRATE? ?
S6	79151	PAD OR PADS OR WIRE () BONDING? ? OR INTERCONNECTION? ? OR INTER () CONNECTION? ?
S7	3576	ELECTRICAL?? () CONNECT???? OR CONNECT???? () POINT? ?
S8	596	S2 (3N) S3 AND S6
S9	10	S8 AND S1
S10	329	S4 OR S5
S11	82332	S6 OR S7
S12	118	S10 AND S11
S13	2	S12 AND S1
S14	10	S13 OR S9
S15	462067	TRANSISTOR? ? OR DIODE? ? OR AMPLIFIER? ? OR SWITCH??
S16	305020	INDUCTOR? ? OR CAPACITOR? ? OR RESISTOR? ? OR FILTER? ? OR DIPLEXER? ?
S17	137	(S15 OR S16) AND (S8 OR S12)
S18	18	S17 AND (ACTIVE OR PASSIVE)
S19	8	S17 AND WIRE () BOND????
S20	8	S19 NOT S14
S22	523	(S2 (2N) S3) AND S6
S23	65	(S2 (2N) S3) AND S1
S24	56	S23 NOT (S9 OR S19)
S25	48	S24 AND PY=1985:2004
S26	22	S24 AND PY=1999:2004
S27	26	S25 NOT S26
S28	118842	WIRE () BOND???? OR WIRE OR WIRING? ? OR WIRES OR WIRED
S29	7272	S2 (2N) S3
S30	7359	S29 OR S4 OR S5
S31	227	S30 AND S28
S33	58	S31 AND (S1 OR S15 OR S16)
S34	51	S33 NOT (S24 OR S14 OR S19)
S35	21	S34 AND PY=1995:2004
S36	0	S31 AND S1 AND S15 AND S16
S37	8	S31 AND (S1 OR (S15 AND S16))
S38	4	S37 NOT (S24 OR S14 OR S19)
S39	419	S28 (3N) (ACTIVE OR PASSIVE)
S40	17	S39 AND S15 AND S16
S41	17	S40 NOT (S24 OR S14 OR S19 OR S38)

Reconnected in file OS 26jul06 11:41:02

SYSTEM:OS - DIALOG OneSearch

File 34:SciSearch(R) Cited Ref Sci 1990-2006/Jul W3

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File 434:SciSearch(R) Cited Ref Sci 1974-1989/Dec

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Set	Items	Description
S1	16770	ACTIVE AND PASSIVE
S2	494704	CHIP? ? OR MICROCHIP? ? OR MICRO () CHIP? ? OR DIE OR DIES OR SUBSTRATE? ? OR WAFER? ?
S3	57	INTRACHIP? ? OR INTRADIE? ? OR INTRAWAFER? ? OR INTRASUBST- RATE? ?
S4	49	INTRA () CHIP? ? OR INTRA () DIE? ? OR INTRA () WAFER? ? OR INTRA () SUBSTRATE? ?
S5	158449	TRANSISTOR? ? OR DIODE? ? OR AMPLIFIER? ?
S6	31561	INDUCTOR? ? OR CAPACITOR? ? OR RESISTOR? ? OR DIPLEXER? ?
S7	1	S1 AND S2 AND (S3 OR S4)
S8	2	(S3 OR S4) AND S5 AND S6
S9	2	S8 NOT S7
S10	1	S1 AND (S3 OR S4)
S11	0	S1 AND S2 AND S3 AND S4
S12	20	S1 AND S2 AND S5 AND S6
S13	2	S12 AND (INTRA OR SAME OR WITHIN)



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wire-bonding AND chip AND (intra-substrate) AND ("fli

Search

☒ Journal sources ☒ Preferred Web sources ☒ Other Web sources ☐ Exact phrase

Searched for:: :All of the words: **wire-bonding AND chip AND (intra-substrate) AND ("flip-chip bonding")**

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- ☐ 1. [TOC.doc \[PDF-237K\]](#)
Jan 2003
...fabricated and flip-**chip** bonded directly...27 2.4.1 **Chip-to-Chip** Demonstrations...112
A.5 **Flip-Chip Bonding**...118 A.6 **Substrate** and Etch Stop Removal...Illustration of a
typical **flip-chip bonding** process...
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- ☐ 2. [Fabrication and characterization of compound semiconductor devices and their electrical and thermal simulation](#)
Mehandru, Rishabh., Jan 2004
Thesis (Ph. D.)--University of Florida, 2004. Title from title page of source document.
Document formatted into pages; contains 174 pages. Includes vita. Includes
bibliographical references.
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- ☐ 3. [Microsoft PowerPoint - EE7356-05 IC manufacturing \[PDF-11K\]](#)
Sep 2004
...VLSI design and lab 21 **Intra-Layer Design Rule Origins**...Active active areas on/in
substrate (poly gates, transistor...VLSI design and lab 25 **Intra-Layer Design Rules**
Metal2...Inverter Layout A A' n p-**substrate** Field Oxide p+ n+ In Out...removal
Economical: Cheap The **chip** is assembled into a package...contact leads for the **chip**. A
wire-bonding machine attaches wires...VLSI design and lab 34 **Flip-Chip Bonding**
Solder bumps **Substrate**...
[http://enr.smu.edu/~pgui/class_notes_pdf/EE7356-05%20...]
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- ☐ 4. [No Slide Title \[PDF-7K\]](#)
Nov 2003
...source and drain regions and **substrate** contacts Create contact...p-epi (a) Base
material: p+ **substrate** with p-epi layer N p+ p-epi...Electrical Engineering **Intra-Layer**
Design Rules Metal2...Layer 1 3 3 2 2 2 Well **Substrate** Select 3 5 Department
of...Electrical Engineering **Bonding** Techniques Lead Frame **Substrate** Die Pad **Wire**
Bonding Department of Computer...Electrical Engineering **Flip-Chip Bonding** Solder
bumps **Substrate**...
[<http://userpages.umbc.edu/~padmanab/fall03/cmpe691a/fa...>]
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wire-bond AND (passive AND active AND substrate) AN

Search

☒ Journal sources ☒ Preferred Web sources ☒ Other Web sources ☐ Exact phrase

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- ☐ 1. [Switchmode Power Supply Miniaturization with Emphasis](#) [PDF-332K]
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...Emphasis on Integrated **Passive Components** on Prefired High Performance Ceramic **Substrates** by Richard W. Hoagland...Emphasis on Integrated **Passive Components** on Prefired High...work. Thick film **passive components** (capacitors and...
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- ☐ 2. [Japan Jisso Technology Roadmap 1999](#) [PDF-939K]
Sep 2000
...components (semiconductors, **passive components**, and printed wiring boards...products, semiconductor devices, **passive components**, and printed wiring boards...components (semiconductors, **passive components**, printed wiring boards), to...
[<http://www.sematech.org/docubase/document/3950beng.pdf>]
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- ☐ 3. [Tummala.layout](#) [PDF-43K]
Dec 1999
...ext-generation **electronic packaging** must be consistent...been mostly **passive** containers...generation in **electronic packaging** education...DIPs) and **wire bond** in the 1970s...miniaturization of **passive components** (Fig. 4...1999) 113 **ELECTRONIC PACKAGING RESEARCH**...integration of **passive** and optoelectronic...types of **active** and **passive components** to 1 type...connection **Wire bond Wire bond**...
[more hits from](#) [<http://techdigest.jhuapl.edu/td2001/Tummula.pdf>]
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- ☐ 4. [Adv. Micro., Jan/Feb 2004, Vol. 31 #1 - Complete Magazine Download](#) [PDF-146K]
Jul 2004
...M Iiiilccccrrrrroooooeeellllleeeccccttttrrrroooooonnniilicccssss Microelectronics Inside the Multichip Module, Hybrid, **Electronic Packaging** and Surface Mount Industries Published by IMAPS - International Microelectronics And Packaging Society & Sidney J. Stein...
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- ☐ 5. [New Online Submission Process for Transactions Papers](#) [PDF-99K]
Sep 2001
...Technologies and they call it Multichip Integral **Substrate** PGA Package Solution (MIPPS) Multilayer...limitations of large size by integrating the **passives** into the

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